WE CLAIM:

1. A clock generation circuit, comprising:

a phase-locked loop for generating a plurality of clock phases;

a first frequency synthesis circuit, comprising:

a first multiplexer, for forwarding a selected one of the plurality of clock phases responsive to a first select signal;

a second multiplexer, for forwarding a selected one of the plurality of clock phases responsive to a second select signal;

a first adder leg, having an input for receiving a frequency select word having an integer portion and a fractional portion, for generating the first select signal corresponding to an accumulation of the frequency select word;

a second adder leg, having an input for receiving a portion of the frequency select word, for generating the second select signal corresponding to a sum of the portion of the frequency select word with an accumulation of the frequency select word;

a toggle multiplexer, having first and second inputs coupled to the outputs of the first and second multiplexers, for toggling a selection of its inputs in sequence; and

a multivibrator, having a clock input coupled to an output of the toggle multiplexer, for inverting an output of the multivibrator responsive to a transition at its clock input.

2. The circuit of claim 1, wherein the first adder leg comprises:

a first adder, for adding a frequency select value having an integer portion and a fractional portion to a feedback value;

a first register for storing a sum from the first adder having an integer portion and a fractional portion; and

a second register, coupled to the first register, for storing the integer portion of the sum, and for presenting its contents to the first multiplexer as the first select signal.

3. The circuit of claim 2, wherein the second adder leg comprises:

a second adder, for adding a portion of the frequency select value with the contents of the first register;

a third register, for storing a sum from the second adder; and

a fourth register, coupled to the third register, for presenting its contents to the second multiplexer as the second select signal.

4. The circuit of claim 1, wherein the select input of the toggle multiplexer is coupled to a first output of the multivibrator.

5. The circuit of claim 4, wherein the multivibrator has a second output that presents a second clock signal complementary to a first clock signal generated at its first output;

wherein each of the first, second, and third registers are clocked by the second clock signal;

and wherein the fourth register is clocked by the first clock signal.

6. The circuit of claim 1, further comprising:

a third multiplexer, for forwarding a selected one of the plurality of clock phases responsive to a third select signal, the third multiplexer having an output coupled to an input of the toggle multiplexer;

a third adder leg, having an input for receiving a portion of the frequency select word, for generating the third select signal corresponding to a sum of the portion of the frequency select word with an accumulation of the frequency select word; and

a clock control circuit, for controlling the toggle multiplexer according to a sequence of select signals.

7. The circuit of claim 6, wherein the first adder leg comprises:

a first adder, for adding a frequency select value having an integer portion and a fractional portion to a feedback value;

a first register for storing a sum from the first adder having an integer portion and a fractional portion; and

a second register, coupled to the first register, for storing the integer portion of the sum, and for presenting its contents to the first multiplexer as the first select signal;

wherein the second adder leg comprises:

a second adder, for adding a portion of the frequency select value with the contents of the first register;

a third register, for storing a sum from the second adder; and

a fourth register, coupled to the third register, for presenting its contents to the second multiplexer as the second select signal;

and wherein the third adder leg comprises:

a third adder, for adding a portion of the frequency select value with the contents of the first register;

a fifth register, for storing a sum from the third adder; and

a sixth register, coupled to the fifth register, for presenting its contents to the second multiplexer as the third select signal.

8. The circuit of claim 1, further comprising:

a second frequency synthesis circuit, comprising:

a first multiplexer, for forwarding a selected one of the plurality of clock phases responsive to a first select signal;

a second multiplexer, for forwarding a selected one of the plurality of clock phases responsive to a second select signal;

a first adder leg, having an input for receiving a frequency select word having an integer portion and a fractional portion, for generating the first select signal corresponding to an accumulation of the frequency select word;

a second adder leg, having an input for receiving a portion of the frequency select word, for generating the second select signal corresponding to a sum of the portion of the frequency select word with an accumulation of the frequency select word;

a toggle multiplexer, having first and second inputs coupled to the outputs of the first and second multiplexers, for toggling a selection of its inputs in sequence; and

a multivibrator, having a clock input coupled to an output of the toggle multiplexer, for inverting an output of the multivibrator responsive to a transition at its clock input;

wherein the first and second adder legs of the first frequency synthesis circuit receive a first initialization value, and are enabled by a first enable signal so that, when the first enable signal is inactive, the first frequency synthesis circuit generates a signal at the output of its multivibrator responsive to a first selected clock phase corresponding to the first initialization value;

and wherein the first and second adder legs of the second frequency synthesis circuit receive a second initialization value, and are enabled by a second enable signal so that, when the second enable signal is inactive, the second frequency synthesis circuit generates a signal at the output of its multivibrator responsive to a second selected clock phase corresponding to the second initialization value.

9. The circuit of claim 8, further comprising:

a first enable multivibrator, for receiving a general enable signal at a data input and receiving the output of the first frequency synthesis circuit at its clock input, for generating the first enable signal responsive to the general enable signal and to a transition of the output of the multivibrator of the first frequency synthesis circuit; and

a second enable multivibrator, receiving the first enable signal at a data input, and receiving the output of the multivibrator of the second frequency synthesis circuit at its clock input, for generating the second enable signal at an output responsive to the first enable signal and to a transition of the output of the multivibrator of the second frequency synthesis circuit.

10. The circuit of claim 9, wherein the second frequency synthesis circuit further comprises:

an enable multiplexer, having a first input coupled to the output of the multivibrator of the second frequency synthesis circuit, having a second input coupled to receive the output of the multivibrator of the first frequency synthesis circuit, having an output coupled to the data input of the multivibrator of the second frequency synthesis circuit, and having a select input coupled to receive the first enable signal so that the output of the multivibrator of the first frequency synthesis circuit is applied to the data input of the multivibrator of the second frequency synthesis circuit responsive to the first enable signal being inactive.

11. The circuit of claim 1, wherein the phase-locked loop comprises:

a phase detector having a first input receiving a reference signal and a second input receiving a feedback signal, for producing an error signal at an output corresponding to a phase difference between the reference and feedback signals;

a filter for low-pass filtering the error signal;

a voltage-controlled oscillator for generating the plurality of clock phases at a frequency selected by the filtered error signal, wherein one of the plurality of clock phases is coupled to the phase detector as the feedback signal.

12. The circuit of claim 11, wherein the voltage-controlled oscillator comprises:

an even-numbered plurality of differential stages, each differential stage having positive and negative inputs and positive and negative outputs;

wherein, the positive and negative outputs of all but a selected one of the plurality of differential stages are connected to the negative and positive inputs, respectively, of the next adjacent one of the plurality of differential stages;

and wherein the positive and negative outputs of the selected one of the plurality of differential stages are connected to the positive and negative inputs, respectively, of the next adjacent one of the plurality of differential stages.

13. A method of synthesizing one or more clock signals of a selected frequency and phase, comprising the steps of:

generating a plurality of clock phases from a phase-locked loop;

adding a first frequency select value including an integer portion and a fraction portion with a feedback value corresponding to a previous result of the adding step, and storing the result in a first register having an integer portion and a fraction portion;

selecting a first one of the plurality of clock phases according to the value of the integer portion of the first register;

adding a portion of the first frequency select value with the feedback value and storing the result in a second register;

selecting a second one of the plurality of clock phases according to the contents of the second register;

applying the first and second selected ones of the plurality of clock phases to inputs of a toggle multiplexer;

selecting the inputs of the toggle multiplexer in a sequence; and

toggling a flip-flop responsive to a transition of the clock phase at the selected input of the toggle multiplexer, to generate the clock signal.

14. The method of claim 13, wherein the step of selecting the inputs of the toggle multiplexer comprises:

applying the clock signal to a select input of the toggle multiplexer, so that the first and second inputs of the toggle multiplexer are selected according to the logic level of the clock signal.

15. The method of claim 13, further comprising:

adding another portion of the first frequency select value with the feedback value and storing the result in a third register;

selecting a third one of the plurality of clock phases according to the contents of the third register; and

applying the third selected ones of the plurality of clock phases to an input of the toggle multiplexer.

16. The method of claim 13, further comprising:

setting first and second enable signals to an inactive state;

responsive to the first enable signal being inactive, in a first frequency synthesis circuit, selecting the first and second ones of the plurality of clock phases responsive to a first initialization value;

in a second frequency synthesis circuit, and responsive to the second enable signal being inactive:

selecting third and fourth one of the plurality of clock phases responsive to a second initialization value, and applying the selected third and fourth ones of the plurality of clock phases to inputs of a second toggle multiplexer;

selecting the inputs of the second toggle multiplexer in a sequence; and

toggling a second flip-flop responsive to a transition of the clock phase at the selected input of the toggle multiplexer of the first frequency synthesis circuit, to generate a phase-shifted clock signal.

17. The method of claim 16, further comprising:

in the first frequency synthesis circuit, then performing the adding, selecting, and applying steps responsive to the first enable signal making a transition from inactive to active; and

in the second frequency synthesis circuit:

adding the frequency select value with a feedback value corresponding to a previous result of the adding step, and storing the result in a third register having an integer portion and a fraction portion;

selecting a third one of the plurality of clock phases according to the value of the integer portion of the third register;

adding a portion of the frequency select value with the feedback value and storing the result in a fourth register;

selecting a fourth one of the plurality of clock phases according to the contents of the fourth register;

applying the third and fourth selected ones of the plurality of clock phases to inputs of a second toggle multiplexer;

selecting the inputs of the second toggle multiplexer in a sequence; and

toggling the second flip-flop responsive to a transition of the clock phase at the selected input of the second toggle multiplexer, to generate the phase-shifted clock signal.

18. The method of claim 17, further comprising:

driving the second enable signal to an active state, responsive to the first enable signal making a transition to the active state.

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